**Miscellaneous IPs**

1. zynq\_ultra\_ps\_e\_0
   1. The Zynq processor IP is responsible for controlling all IPs and how they interact with each other. This IP is self-explanatory but acts as the brains of the control signal for the entire design. The ARM processor clock is set to run at a max frequency of 1.334 GHz within the clock configuration window (Full Power Domain Clocks → Processor/Memory clocks → ACPU). Though the requested frequency is 1.334 GHz, the reported actual frequency is 1.2 GHz. This speed is necessary for receiving data from the Python script on the PC as fast as possible, while also converting the pixel data from integers to floating-point numbers as fast as possible. The IP also generates a pl\_clk of 150 MHz. The pl\_clk is the output clock that is responsible for the synchronization of all of the IPs that are contained within the programmable logic (PL) or FPGA fabric. It is set to 150 MHz in the clock configuration window (Low Power Domain Clocks) because that is the fastest clock speed that our floating-point functions can operate within the Gamma\_Imp\_0, GradientsMulti\_1, and SubsetCoordsMulti\_0 IPs. The entire design is kept on this clock to remain synchronous for simplicity. \*NOTE: it may be possible to build the design asynchronously, but there is a potential conflict with URAM as it does not support true dual porting with separate clocks. The Zynq IP has two PS-PL master interfaces that are defined within it; AXI HPM0 FPD, and AXI HPM1 FPD. These two signals are responsible for controlling both of the AXI interconnects that are defined with the design.
2. rst\_ps8\_0\_100M
   1. The Processor System Reset is the primary reset for all IPs in the design. The reset wire comes from the zynq\_ultra\_ps\_e\_0. This IP was autogenerated by Vivado and may not be necessary within the final design. No settings were modified inside the IP, so it does not perform any special task. The Zynq reset wire may be just as capable to reset all IPs as the reset that the Processor System Reset IP produces. However, it did not cause a conflict so it was left alone.
3. axi\_interconnect\_0
   1. The primary interconnect for all memory modules within the design. This interconnect lets the processor control and access all AXI BRAM Controllers that are used within the echo.c server to write and read data as needed from the individual BRAMs.
4. axi\_interconnect\_1
   1. The primary interconnect for all custom IPs within the design. This interconnect lets the processor control and access all custom IPs that were created to support the AXI Interface. Each (all) IPs that have AXI support come with 4 AXI Slave registers that are used within the echo.c server to write and read data as needed from the individual IPs.
5. Counter\_0
   1. This IP was created solely for debugging and is not totally necessary within the design. A simple counter that is used as a timer to time the gradients and gamma IPs execution time and to verify that the IPs have started processing. This IP is not discussed as a standalone IP document.
6. VIO
   1. Used as the primary debugging tool within the FPGA fabric. Monitors signals of outputs/inputs to/from IPs
   2. Clock wizard
      1. Used to set the clock to the VIO to 150 MHz so its equal to the rest of the clocks in the fabric.
   3. Programmable Differential Clock
      1. Used as a “free-running clock” to get rid of a bug where the VIO wouldn’t appear in the Vivado hardware manager tool.